REMARKS

Claims 2-3, 7, and 17-21 were pending when last examined. All pending claims are shown in the detailed listing above.

Claim Rejections – 35 USC § 102

Claim 2 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Corsi (US 5,912,551). Applicants respectfully traverse.

The Examiner states:

> Applicant argues Corsi does not disclose an algorithm generator distinct from the duty cycle generator, digital counter and first comparator. However, Applicant's claim language does not require the algorithm generator be distinct from the duty cycle generator, digital counter and first comparator. The claim language algorithm generator is broad and only requires production of an algorithm, such as the controller disclosed by Corsi.

Office Action, p. 2. Applicants respectfully disagree.

The Examiner essentially ignores the limitation of "algorithm generator" in claim 2 and reads the claim as "the duty cycle generator, the digital counter and the first comparator producing an algorithm that determines the rate of change for modifying the duty cycle." But that is not the claim at hand.

Applicants' claim 2 expressly recites "an algorithm generator" which is not the same as the duty cycle generator, digital counter, and first comparator. Claim 2 could not be any more clear. This is not a case where the Applicant seeks to distinguish the claim over the prior art by arguing limitations not present in the claim. Claim 2 already includes the limitation of the "algorithm generator." Thus, Examiner's assertion that "Applicants' claim language does not require the algorithm generator be distinct from the duty cycle generator, digital counter and first comparator" is baseless. It is inappropriate for the Examiner to not consider the actual limitations of claim 2.

Because the Examiner's rejection of claim 2 is based on a reading which ignores limitations of the claim, such rejection cannot stand.

The Examiner also states:

> Applicant further argues Corsi does not disclose an algorithm that determines the rate of change of modifying the duty cycle. However, since duty cycle is controlled, the rate of change of the duty cycle is controlled, therefore the rate of change of modifying the duty cycle must be determined.

Office Action, p. 2. Applicants respectfully disagree.

The Examiner's argument is based on a flawed assumption. In particular, the Examiner assumes that just because the duty cycle is modified in Corsi, there must necessarily be a change in the rate at which the duty cycle is modified. That is not only illogical, but it is simply not true. Corsi simply does not disclose or teach anything about "adjusting the rate of change for modifying the duty cycle" as recited in claim 2. Thus, there is no reason why Corsi would need or be motivated to "determine[] the rate of change for modifying the duty cycle" as recited in claim 2. Accordingly, claim 2 is not anticipated by Corsi.

For at least the reasons discussed above, Applicants respectfully request that the rejection of claim 2 under 35 U.S.C. § 102(b) as being anticipated by Corsi be withdrawn and this claim be allowed.

Claims 7 and 17-21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Duffy (US 2002/0171985). Applicants respectfully traverse.

Claim 7 recites *inter alia*, "altering the duty cycle at a first frequency to produce the desired output voltage based upon the indication; and if a change in the load is detected, changing the frequency of alteration of the duty cycle." An example of changing the frequency at which the duty cycle is altered or modified is described in the present Application at paragraph [0035]:

> The system measures both the absolute value of the output voltage and the rate of change of this voltage ("dv/dt"). In the case of a transition to a sudden heavy load, from no load, it is preferred to regulate the voltage more quickly than it would otherwise be regulated by comparator 154. A second comparator 158, with a reference different than the first one, for example 20mV below the first one, detects the heavy load condition and accelerates the active pulse widening. For example, if the second comparator 154 output is zero, the clock frequency to the algorithm generator is 2 μs. Hence the algorithm generator can issue a signal once every 2 μs to up-down counter to increment the duty cycle by one level. On the other hand, if the second comparator 154 output is one, the clock frequency to the algorithm generator is changed to 250nSec, which is 8X faster. This second comparator circuitry greatly reduces the duration and magnitude of a resultant output voltage dip, as is discussed with regard to FIGS. 4 and 5.

Such changing the frequency of alteration of the duty cycle as described in the present Application and claimed in Applicants' claim 7 is not disclosed or taught at Fig. 14 of Duffy.

The Examiner states:

> Applicant argues Duffy does not disclose changing the frequency of alteration of the duty cycle. However, in Fig. 14 at time 1450, Duffy discloses turning on the power transistor uppers before they would turn on at the previous switching frequency up to time 1450. Therefore, Duffy has disclosed changing the frequency of alteration of the duty cycle at time 1450. Duffy has not simply extended the period since the individual phases have continued to discharge. Clearly the frequency of alteration has been changed, since the power transistors have turned on before the period of the old switching frequency has completed.

Office Action, p. 3. Applicants respectfully disagree.

The Examiner's characterization of the disclosure of Duffy is not accurate. Neither Fig. 14 nor the accompanying description in Duffy concerns changing the frequency of alteration of the duty cycle. What Duffy actually describes for Fig. 14 is at paragraph [0078]:

> [0078] In an exemplary embodiment, an ATRH event starts at time 1450 and ends at time 1451. At the start of the ATRH event, all low-side power switches 1220 are turned off and then, after a short delay, e.g., 20

> nanoseconds, all high-side power switches 1210 are turned on causing the previously staggered inductor charging to occur in parallel. See, for example, FIG. 14, reference 1460. At the end of the ATRL event 1451, the inductor charging is returned to its quiescent voltage regulation mode phased switching.

It is clear from this description in Duffy that the frequency illustrated in Fig. 14 is the frequency for turning on and off the switches. The switching frequency of Fig. 14 of Duffy is not the same a "frequency of alteration of the duty cycle" as recited in Applicants' claim 7. No "duty cycle" is shown or described for Fig. 14 of Duffy, much less a "frequency of alteration of the duty cycle." Thus, Duffy does not anticipate claim 7 which includes "altering the duty cycle at a first frequency to produce the desired output voltage based upon the indication; and if a change in the load is detected, changing the frequency of alteration of the duty cycle."

For at least the reasons discussed above, Applicants respectfully request that the rejection of claim 7 under 35 U.S.C. § 102(b) as being anticipated by Duffy be withdrawn and this claim be allowed. Furthermore, because claims 17 and 18 depends from claim 7 and include further limitations, the Applicants respectfully requests that the rejection of these dependent claim under 35 U.S.C. § 102(b) as being anticipated by Duffy also be withdrawn and these claims be allowed.

Similarly, claim 19 has limitations which are not disclosed in Duffy. In particular, claim 19 recites *inter alia*, "monitor circuitry for monitoring the load, wherein the monitor circuitry causes a change in the frequency of altering the duty cycle; wherein if the load increases, the frequency of altering is increased, thereby minimizing a dip in the output voltage." As discussed above, Duffy does not disclose any "frequency of altering the duty cycle," much less "monitor circuitry [which] causes a change in the frequency of altering the duty cycle" and "wherein if the load increases, the frequency of altering is increased." Thus, claim 19 is not anticipated by Duffy.

For at least the reasons discussed above, Applicants respectfully request that the rejection of claim 19 under 35 U.S.C. § 102(b) as being anticipated by Duffy be withdrawn and this claim be allowed. Furthermore, because claims 20 and 21 depend from claim 19 and include further limitations, the Applicants respectfully requests that the rejection of these dependent claims under 35 U.S.C. § 102(b) as being anticipated by Duffy also be withdrawn and these claims be allowed.

Claim Rejections – 35 USC § 102

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Corsi in view of Ogasawara (US 6,377,428).

Claim 3 depends from claim 2, which include limitations not disclosed in Corsi, as discussed above. Nor are such limitations disclosed or taught in Ogasawara, taken alone or in combination with Corsi. Accordingly, claim 3 is not rendered obvious by the cited art.

For at least the reasons discussed above, Applicant respectfully requests that the rejection of claim 3 under 35 U.S.C. § 103(a) be withdrawn and this claim be allowed.

CONCLUSION

Applicants respectfully request that the pending claims be allowed and the case passed to issue. Should the Examiner wish to discuss the Application, it is requested that the Examiner contact the undersigned at (415) 772-7428.

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

3/12/08 Richard A. Pasik

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